AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1-7. (cancelled)

8. (currently amended) A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor with the interlayer dielectric layer being in direct contact with a component of the non-volatile memory transistor,

a wiring layer provided on and in direct contact with the interlayer dielectric layer,

wherein the interlayer dielectric layer includes a first oxide film provided as a lowermost layer of the interlayer dielectric layer, a layer containing nitride provided on and in direct contact with the first oxide film, [[and]] a second oxide film provided on and in direct contact with the layer containing nitride[[.]], the first oxide film is an oxide film that is formed by a reduced pressure CVD method using TEOS, and the first oxide film has a thickness of 30 – 70nm.

9-21. (cancelled)

22. (currently amended) A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor,

a wiring layer provided on and in direct contact with the interlayer dielectric layer,

wherein the interlayer dielectric layer comprises a first oxide film provided as a lowermost layer of the interlayer dielectric layer, a layer containing nitride provided on and in direct contact with the first oxide film, [[and]] a second oxide film provided on and in direct contact with the layer containing nitride[[.]], the first oxide film is an oxide film that is formed by a reduced pressure CVD method using TEOS, and the first oxide film has a thickness of 30-70nm.

23-25. (cancelled)

26. (currently amended) A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor with the interlayer dielectric layer being in direct contact with a component of the non-volatile memory transistor; and

a wiring layer provided on and in direct contact with the interlayer dielectric layer,

wherein the interlayer dielectric layer includes a first oxide film provided as a lowermost layer of the interlayer dielectric layer, a layer containing nitride provided on and in direct contact with the first oxide film, a second oxide film provided on and in direct contact with the layer containing nitride, ~~and the first oxide film is free of boron and phosphorus.~~ the first oxide film is an oxide film that is formed by a reduced pressure CVD method using TEOS, and the first oxide film has a thickness of 30-70nm.

27-29. (cancelled)

30. (currently amended) A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor; and

a wiring layer provided on and in direct contact with the interlayer dielectric layer,

wherein the interlayer dielectric layer comprises a first oxide film provided as a lowermost layer of the interlayer dielectric layer, a layer containing nitride provided on and in direct contact with the first oxide film, a second oxide film provided on and in direct contact with the layer containing nitride, ~~and the first oxide film is free of boron and phosphorus.~~ the first oxide film is an oxide film that is formed by a reduced pressure CVD method using TEOS, and the first oxide film has a thickness of 30-70nm.

31-33. (cancelled)

34. (currently amended) A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor; and

a wiring layer provided on and in direct contact with the interlayer dielectric layer,

wherein the interlayer dielectric layer comprises a first oxide film provided as a lowermost layer of the interlayer dielectric layer, a layer containing nitride provided on and in direct contact with the first oxide film, a second oxide film provided on and in direct contact with the layer containing nitride, [[and]] the first oxide film has a thickness of 30-70nm[[.]], and the first oxide film is an oxide film that is formed by a reduced pressure CVD method using TEOS.

35. (cancelled)